

IRFP17N50L

SMPS MOSFET

HEXFET® Power MOSFET

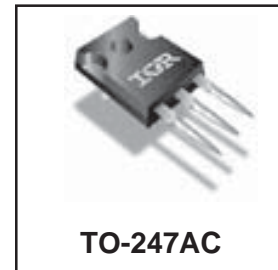
Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications

V _{DSS}	R _{DS(on)} typ.	T _{rr} typ.	I _D
500V	0.28Ω	170ns	16A

Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	16	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	11	
I _{DM}	Pulsed Drain Current ①	64	
P _D @ T _C = 25°C	Power Dissipation	220	W
	Linear Derating Factor	1.8	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ②	13	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	16	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	64		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	
t _{rr}	Reverse Recovery Time	—	170	250	ns	T _J = 25°C, I _F = 16A
		—	220	330		T _J = 125°C, di/dt = 100A/μs ④
Q _{rr}	Reverse Recovery Charge	—	470	710	nC	T _J = 25°C, I _S = 16A, V _{GS} = 0V ④
		—	810	1210		T _J = 125°C, di/dt = 100A/μs ④
I _{RRM}	Reverse Recovery Current	—	7.3	11	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.60	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.28	0.32	Ω	$V_{GS} = 10V, I_D = 9.9A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -30V$
R_G	Internal Gate Resistance	—	1.4	—	Ω	$f = 1\text{MHz}, \text{open drain}$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	11	—	—	S	$V_{DS} = 50V, I_D = 9.9A$
Q_g	Total Gate Charge	—	—	130	nC	$I_D = 16A$ $V_{DS} = 400V$ $V_{GS} = 10V$, See Fig. 7 & 15 ④
Q_{gs}	Gate-to-Source Charge	—	—	33		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	59		
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	$V_{DD} = 250V$ $I_D = 16A$ $R_G = 7.5\Omega$ $V_{GS} = 10V$, See Fig. 14a & 14b ④
t_r	Rise Time	—	51	—		
$t_{d(off)}$	Turn-Off Delay Time	—	50	—		
t_f	Fall Time	—	28	—		
C_{iss}	Input Capacitance	—	2760	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$, See Fig. 5 $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤
C_{oss}	Output Capacitance	—	325	—		
C_{rss}	Reverse Transfer Capacitance	—	37	—		
C_{oss}	Output Capacitance	—	3690	—		
C_{oss}	Output Capacitance	—	84	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	159	—		
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	120	—		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ④	—	390	mJ
I_{AR}	Avalanche Current ④	—	16	A
E_{AR}	Repetitive Avalanche Energy ④	—	22	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.56	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 3.0\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 16A$. (See Figure 12).
- ③ $I_{SD} = 16A$, $di/dt \leq 347A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

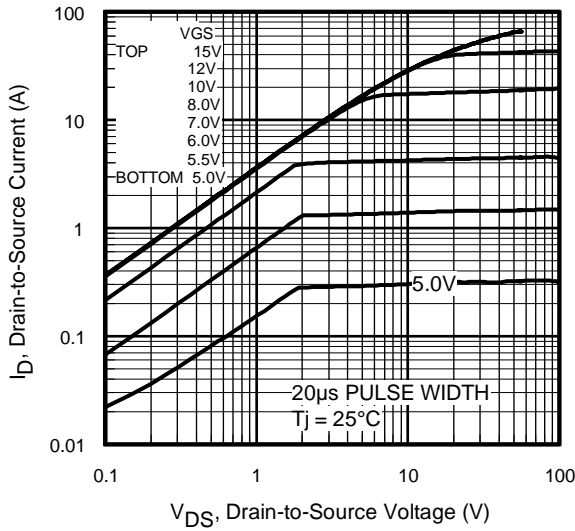


Fig 1. Typical Output Characteristics

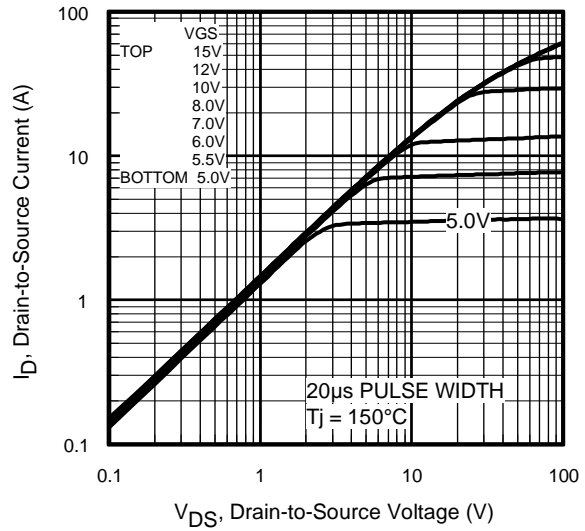


Fig 2. Typical Output Characteristics

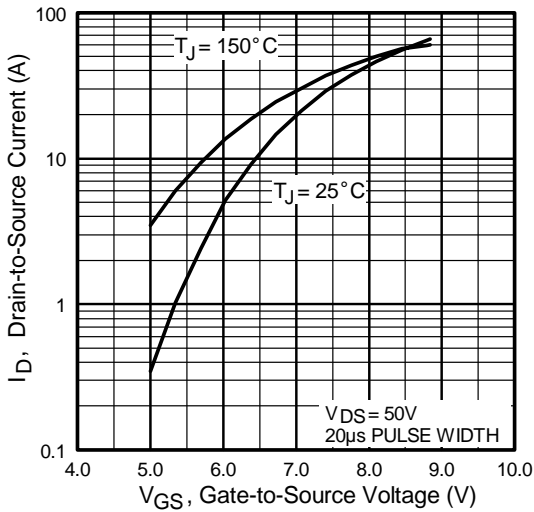


Fig 3. Typical Transfer Characteristics

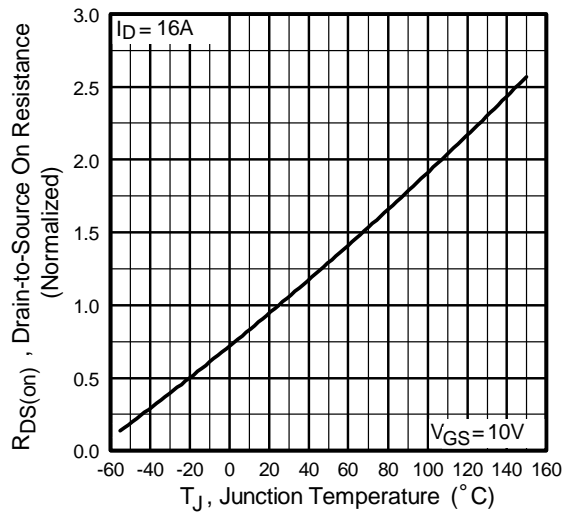


Fig 4. Normalized On-Resistance Vs. Temperature

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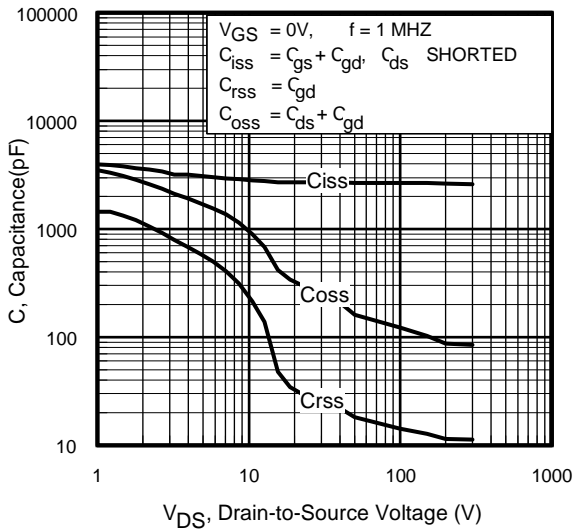


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

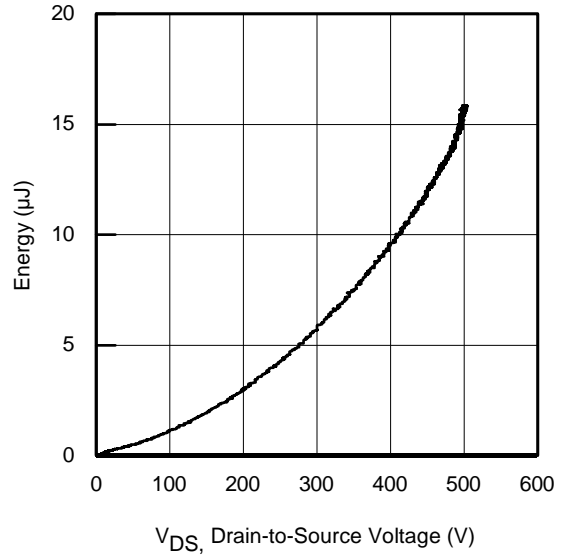


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

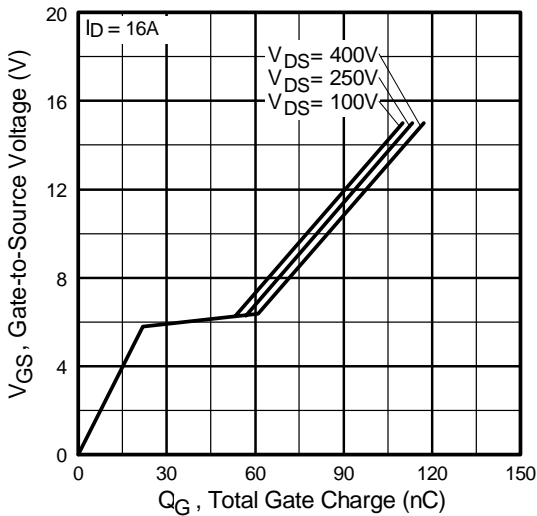


Fig 7. Typical Gate Charge Vs. Gate-to-Source Voltage

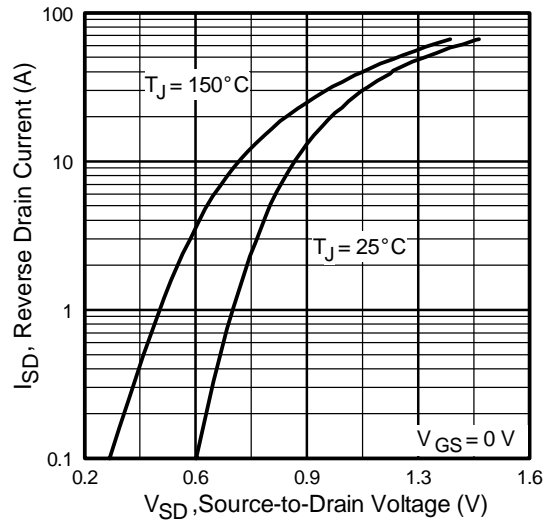


Fig 8. Typical Source-Drain Diode Forward Voltage

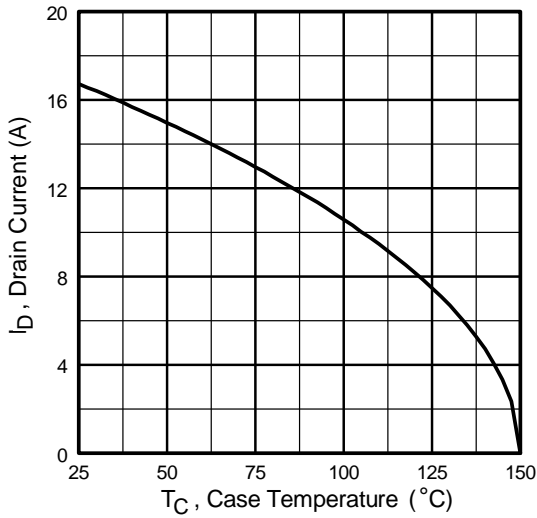


Fig 9. Maximum Drain Current Vs. Case Temperature

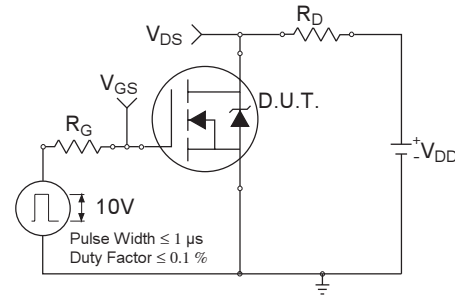


Fig 10a. Switching Time Test Circuit

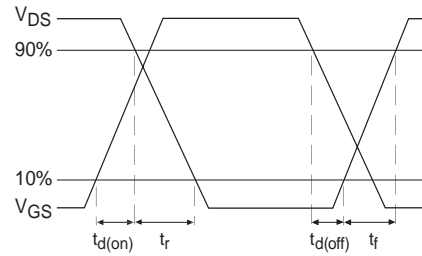


Fig 10b. Switching Time Waveforms

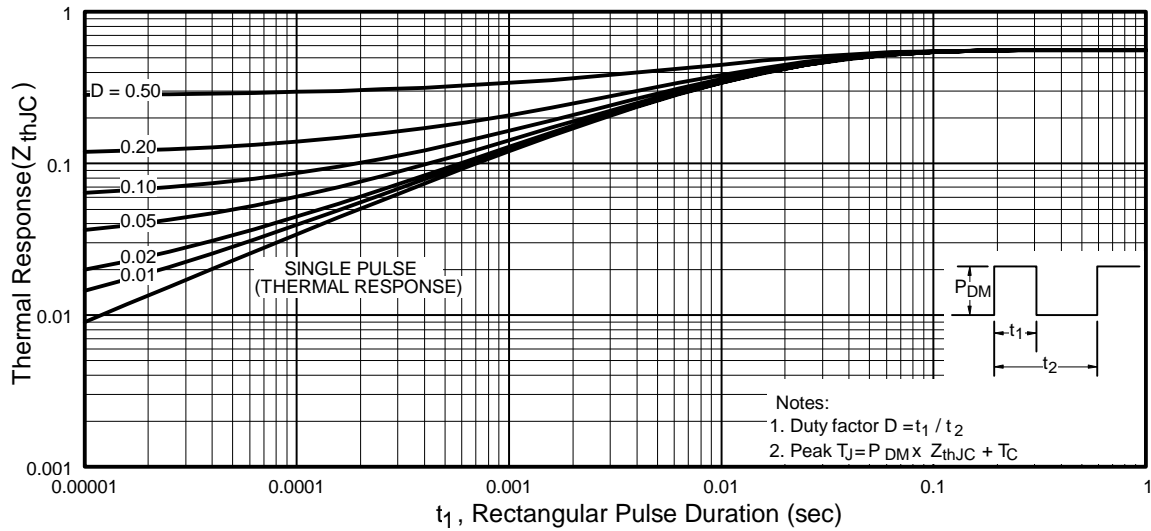


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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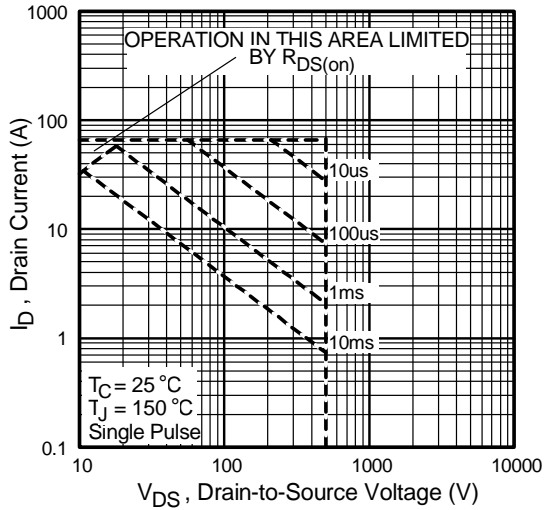


Fig 12. Maximum Safe Operating Area

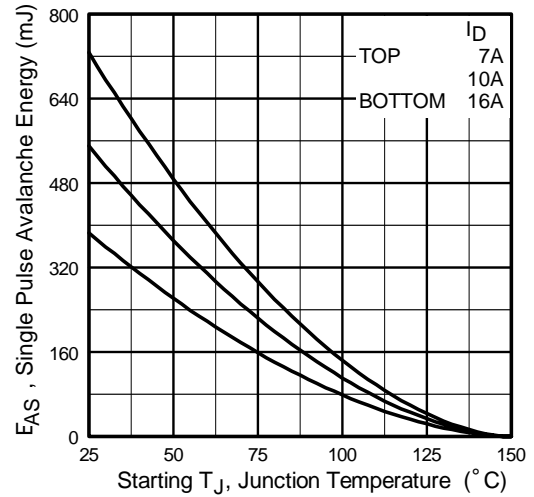


Fig 13. Maximum Avalanche Energy vs. Drain Current

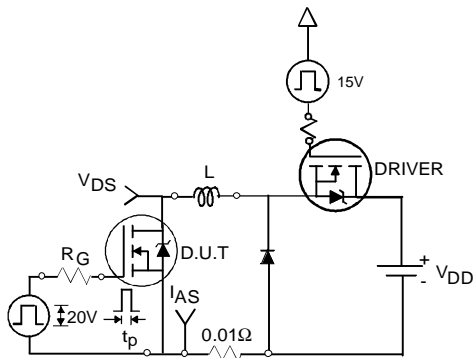


Fig 14a. Unclamped Inductive Test Circuit

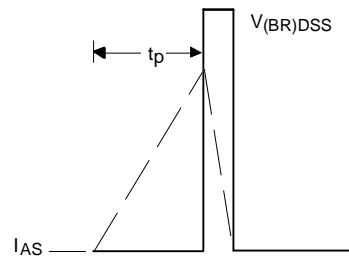


Fig 14b. Unclamped Inductive Waveforms

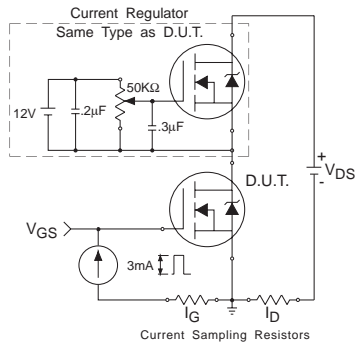


Fig 15a. Gate Charge Test Circuit

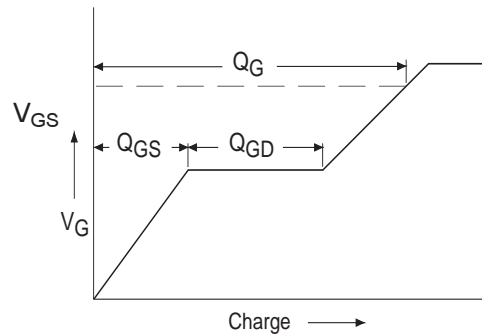
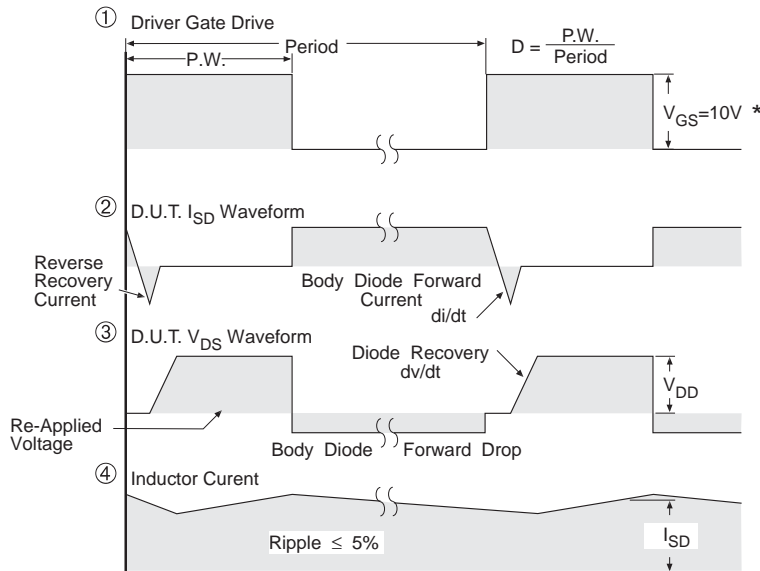
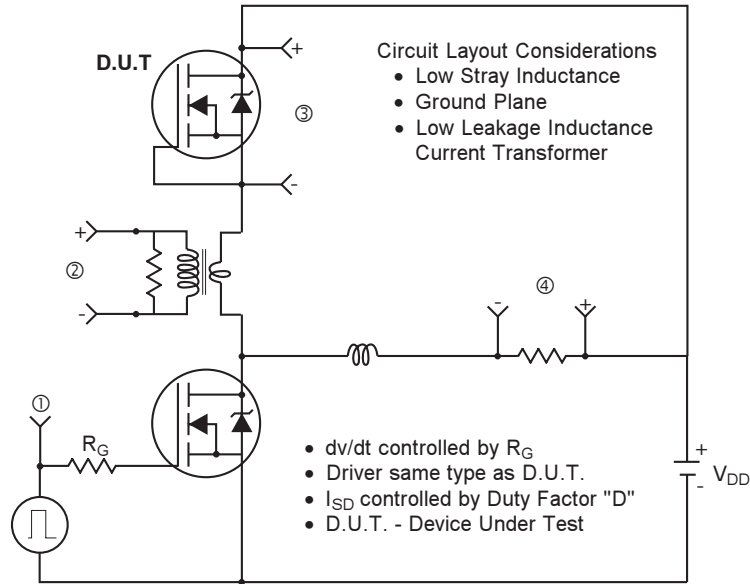


Fig 15b. Basic Gate Charge Waveform
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Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

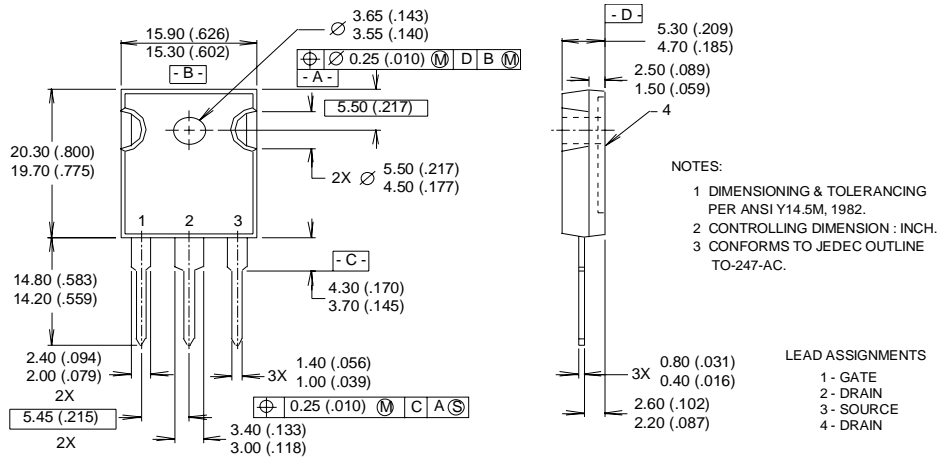
Fig 16. For N-Channel HEXFET® Power MOSFETs

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TO-247AC Package Outline

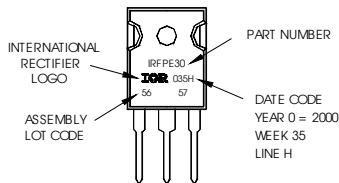
Dimensions are shown in millimeters (inches)



TO-247AC Part Marking Information

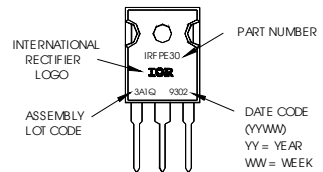
Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFP30
 WITH ASSEMBLY
 LOT CODE 5657
 ASSEMBLED ON WW 35, 2000
 IN THE ASSEMBLY LINE "H"



Notes: This part marking information applies to devices produced before 02/26/2001 or for parts manufactured in GB.

EXAMPLE: THIS IS AN IRFP30
 WITH ASSEMBLY
 LOT CODE 3A1Q



TO-247AC package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Automotive [Q101] market.
 Qualification Standards can be found on IR's Web site.

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